

WEST

Generate Collection

Print

L1: Entry 2 of 3

File: TDBD

Oct 1, 1973

TDB-ACC-NO: NN73101362

DISCLOSURE TITLE: Complementary FET Devices Having Composite Gate Dielectric and Composite Gate Electrode Structures. October 1973.

PUBLICATION-DATA:

IBM Technical Disclosure Bulletin, October 1973, US

VOLUME NUMBER: 16

ISSUE NUMBER: 5

PAGE NUMBER: 1362 - 1363

PUBLICATION-DATE: October 1, 1973 (19731001)

CROSS REFERENCE: 0018-8689-16-5-1362

DISCLOSURE TEXT:

2p. Prior complementary field-effect transistor (FET) devices employ aluminum-silicon nitride-silicon oxide gate structures. Such gate structures are subject to three disadvantages, i.e., the P-channel FET exhibits high-threshold voltage, the N-channel FET exhibits low-threshold voltage, and both P and N-channel FETs are subject to significant threshold voltage shift in response to temperature-bias stressing. - The foregoing disadvantages are avoided by employing an aluminum, P-doped polycrystalline silicon, oxygen annealed silicon nitride, thermal oxide gate structure. A P-doped polycrystalline silicon gate has a more positive gate-to-substrate work function than an aluminum gate. Therefore, with everything else equal, N-channel FETs with an aluminum silicon gate have a substantially higher threshold voltage than N-channel aluminum gate FETs. The corresponding P-channel devices have a much lower threshold voltage than aluminum gate P-channel FETs. The oxygen annealing of the silicon nitride layer improves the threshold voltage stability of both the P and N-channel FETs. - The complementary FET devices shown in the drawing are fabricated as follows: P diffusions 1 and 2 are made in N substrate 3, N diffusions 4 and 5 are made in P pocket 6 formed within substrate 3, and thick oxide 7 is formed in a conventional manner. The thick oxide is etched away in the device channel area and relatively thin gate oxide 8 is regrown. Silicon nitride 9 is deposited on the gate oxide and then subjected to an oxygen annealing step, for example, at 1050 degrees C for one hour using dry O₂. Polycrystalline silicon 10 is deposited on the oxidized nitride layer and is P-doped either by subsequent diffusion or simultaneously with the deposition of the polysilicon. A thin layer of thermal oxide is then grown on the polycrystalline silicon in order to improve photoresist adherence. Contact photoresist is applied and windows are opened in the composite layer consisting of thin silicon oxide, polycrystalline silicon, silicon nitride and thick oxide layer 7. Aluminum is deposited and is subtractively etched along with the polysilicon. Finally, the entire structure is sintered.

SECURITY: Use, copying and distribution of this data is subject to the restrictions in the Agreement For IBM TDB Database and Related Computer Databases. Unpublished - all rights reserved under the Copyright Laws of the United States. Contains confidential commercial information of IBM exempt from FOIA disclosure per 5 U.S.C. 552(b)(4) and protected under the Trade Secrets Act, 18 U.S.C. 1905.

COPYRIGHT STATEMENT: The text of this article is Copyrighted (c) IBM Corporation 1973. All rights reserved.

BEST AVAILABLE COPY

02/23/2003, EAST Version: 1.03.0002